

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Leonard Forbes et al.

Title:

TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND

USE

Docket No.:

303.324US2

Filed:

February 23, 1999

Examiner:

Michael Trinh

Serial No.: 09/256,643

Due Date: November 23, 2001

Group Art Unit: 2822

Commissioner for Patents Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

 \underline{X} A return postcard.

X An Amendment and Response under 37 CFR 1.111 (7 Pages).

 \underline{X} Petition for Extension of Time (1 pg.)

 \underline{X} A check in the amount of \$110.00 to cover the Extension of Time Fee.

X A Supplemental Information Disclosure Statement (1 pgs.), Form 1449 (1 pgs.), and copies of 2 cited references.

X A check in the amount of \$180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

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Atty: Robert E. Mates

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<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this <u>21st</u> day of <u>November</u>, 2001.

Name

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Customer Number 21186

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